Data alignment at Stereo Finder

S. Holm 12/27/04
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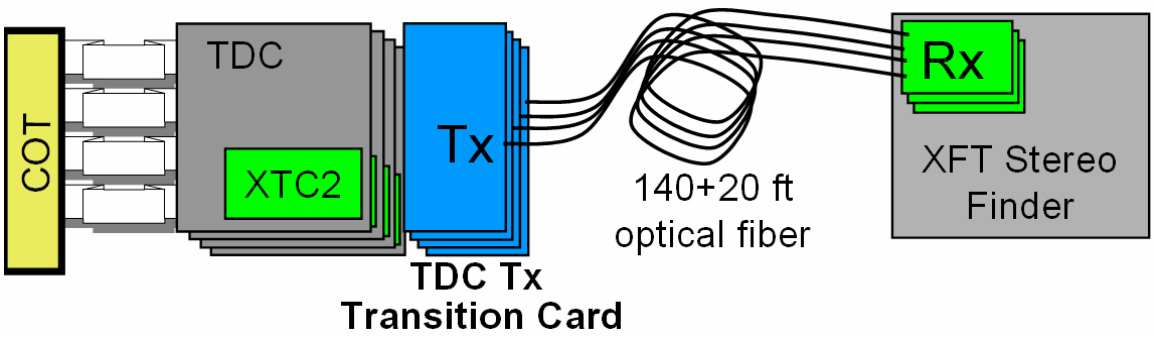
Introduction: In short data is generated at the TDC modules located near the detector, that data represents wire hit information within a 12 wire cell. The parallel wire hit data is sent to a SERDES part to convert to a serial bit stream which is transported over a 160 ft. fiber optic cable to another SERDES part which converts the data back to a parallel format. The Stereo Finder FPGA must align the data from six separate Fibers into an event. Each fiber is used to transport 4 cells worth of hit wire data. Each Finder FPGA can handle 18 cells worth of wire hit data. An event is 396ns, the wire hit data for all 18 cells plus some neighboring cells is collected and then processed within the Stereo Finder FPGA. The wire hit data that is transported on the 6 fibers will all have some latency between them. The Input Alignment section within the Stereo Finder FPGA makes sure that the wire hit data for all 18 cells for a particular event is aligned for the same event. It does this by storing the data being transported on the six fibers into six different FIFOs on certain conditions all operating at there own write clock phase and then reading the data out of all six FIFOs under a particular condition using a universal clock. This allows the data coming out of the FIFOs to be aligned into an event. The aligned data can then be processed by the Stereo Finder algorithim.

A short description on the generation of the data is provided below, a detailed account of the data can be found in the SXFT specification and the TX-RX Mezzanine board specification. The remainder of this note will detail the alignment of the wire data within the Stereo Finder FPGA.

The Wire hit data originates at the detector. A TDC module located near the detector produces 6 bits of data for each of the 12 wires within a cell. This data identifies whether a wire has a “hit” on it for a particular time slice. There are 6 identified time slices within each 396ns period, or 3 CDF_Clock cycles. Each TDC module will cover 8 cells of the detector. In addition to sending up the hit information for each wire, it is desirable to tag the information with a Beam_Zero marker, to identify its position in time as well as some type of identification tag to mark the source of the data. The data from the TDC modules is sent to the Stereo Finder modules via an 8B/10B encoded serial optical bit stream. A XFT2 TDC transition module receives the data from the TDC/XTC combination and transmits the data onto a fiber optic cable which is received at one of three RX Mezzanine boards located on the Stereo Finder board. The XFT2 TDC transition module is located in the TDC crate. A block diagram of the data path is shown below.



See the following documents on the TX/RX board specification:
http://www-ppd.fnal.gov/tshaw.myweb/Xft_upgrade/RX_Mezz/RX_Mezz_Spec.pdf
http://www-cdf.fnal.gov/internal/people/links/NilsKrumnack/xft/spec-09Aug04a.pdf
http://www.hep.uiuc.edu/engin/cdf/xft2/

The Stereo Finder board's Finder FPGA receives the parallel data generated from the RX Mezzanine modules, there are 2 Finder FPGA's with each one capable of receiving data from 6 fibers. Some of the fibers data is shared between the two FPGA's. The Finder FPGA's are expecting data every 16ns in the form of 16 bit words: 12 bits of data, Beam_Zero marker, Time_Zero marker and 2 bit group identifier. The data should come in 24 consecutive slices of XTC2 data, validated by the RX Data Valid signal generated by the TLK1501 Transceiver located on the RX Mezzanine board. Since the XTC2 data is being sent using a 16ns clock there will be an 'idle' word that should come at the beginning or end of a data stream(an event is occurring every 396ns – 16ns is not a multiple of 396ns). The 'idle' word will come 3 out of 4 buckets to make up the difference between the transmitting frequency and the CDF Clock Frequency. The 'idle' word should be only 1 clock tick in length, however the alignment algorithm will allow for more. The 'idle' word is detected by the TLK1501 receiver and the RX Data Valid signal produced will be low with the 'idle' word.

There will be a period of time referred to as an abort gap within the data transmission – an abort gap is 20 CDF_CLOCK(132ns). Invalid(idle) data will come during the abort gaps Events will come between abort gaps.. Approximately 11 events with each event occupying 3 CDF_CLOCKs. In a pattern similar to below:
So the pattern of BCs (in terms of CDF_CLKs) is
3 3 3 3 3 3 3 3 3 3 20
3 3 3 3 3 3 3 3 3 3 20
3 3 3 3 3 3 3 3 3 3 20
Methods are implemented to determine if the data is part of an event or part of the abort gap. The data transported on a fiber during an abort gap should be the idle pattern along with TX_DV = '0' & TX_ER = '0'. The data from the receiver should be the same idle pattern along with RD_DV= '0' and RX_ER = '0'. If an error occurred on the link the RX_ER would be '1'.

There is some latency associated with the TLK1501 Transceiver part located on the XFT2 TDC Transition module and the RX Mezzanine boards; this may cause the data to be misaligned by up to 30ns between the fibers. The 16ns clock that drives the transmitter of the TLK1501 at the XFT2 TDC Transition board and the 16ns clock that is operating the TLK1501 on the RX Mezzanine board are both provided by separate oscillators,

although these Oscillators are all running at the same frequency the phase difference between them can be up to 360 degrees. Therefore another 16ns will need to be accounted for. With the latency and the phase differences there is a possible 46ns of latency between a channels data when it is received by Stereo Finder FPGA(The Input Alignment block will allow for more than double this, basically up to the depth of the FIFO's which is 16.)

The Alignment section's purpose is to provide an events aligned data to the Finder algorithm, aligned to the Stereo Finder FPGA's internal 16.5ns clock which is derived from CDF_CLOCK(132ns) divided by 8. A divide by two function was implemented on the Stereo Finder board to provide a 66ns clock to the Stereo Finder FPGA were it was further divided down by 4 to the 16.5ns required.

The Input Alignment section along with the remainder of the Stereo Finder FPGA will start to function if the Operate Board bit is set, followed by a CDF-HRR sequence followed by a CDF_B0 signal on the backplane. The R/W bit(0) in the Control/Status register of the Finder Board labeled "Operate board" is a requirement to let the board function. The Operate Board register bit will reset if a CDF_RECOVER signal is on the backplane.

The Stereo Finder FPGA's input FIFO's will start to accept data when the Alignment section is enabled via the following conditions:

- Operate Bit along with the HRR & B0 sequence
- Data Valid which is the combination of RX_DV = '1' and RX_ER ='0' provided by the RX mezzanine board.
- First slice of data from the RX mezzanine board has the Time_Zero Marker(bit14) = '1' and Group ID(bit13..12) = "00"

If the above conditions are met then slices of wire information are written to the Input FIFO that is associated with a particular Fiber. The following slices of data of an event are written into the FIFO as long as the RX_DV and RX_ER conditions are met. If RX_DV goes low for a slice, then the data associated with that slice will not be written into the FIFO. Also if a RX_ER signal is present with a slice the data associated with that slice will not be written into the FIFO(this will eventually cause a misalignment when the data is read out and the FIFO's will get reset).

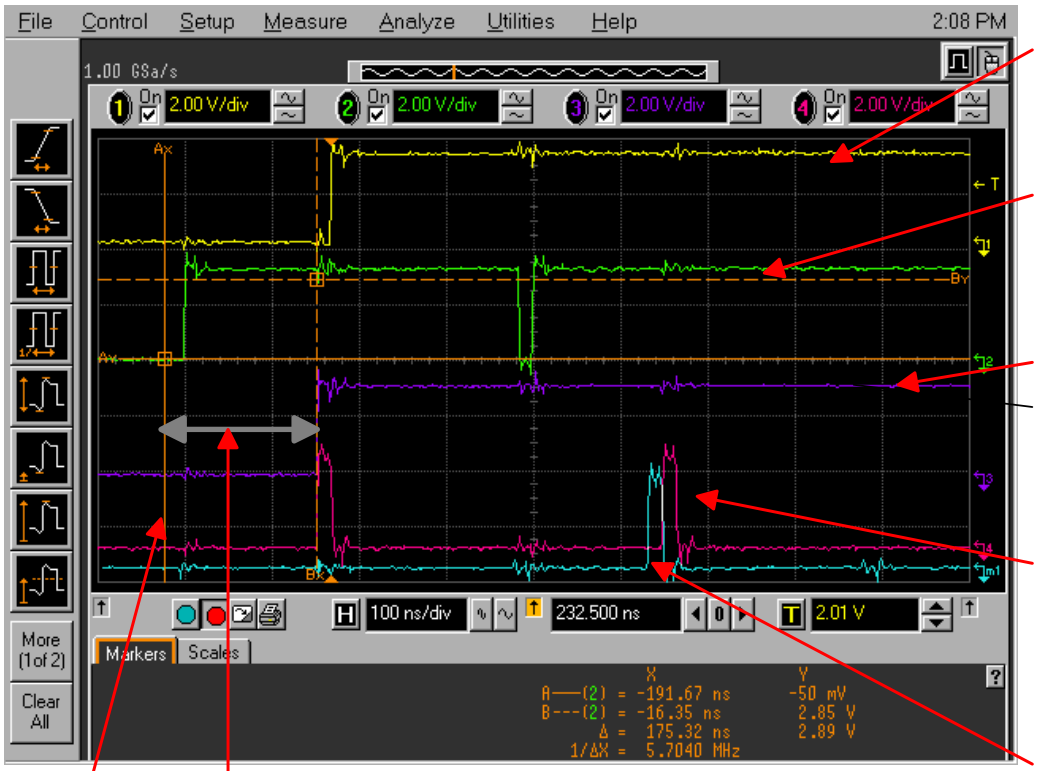
Data is read out of all FIFO's at the same time and aligned to a particular phase of the CDF_CLOCK. The FIFO's will be read every 16.5ns(CDF Clock divided by 8). The read sequence is initiated when all six FIFO's have at least one slice of data written into them. A not empty signal along with a full is generated by the FIFO logic. The not empty flag from all six FIFO's being a '1' will enable the six FIFO's to be read.

An error is generated from the FIFO's logic:
If any of the six FIFO's becomes full before all of them have at least one slice of data, then an error_full bit is set. The error full bit will reset(clear) all the FIFO's and also the routine to allow data to be written to the FIFO. The write routine will become enabled again on the next Time_Zero marker = '1' and Group ID "00" combination. The error_full bit will also set the Error_Links_FE bit which is sent to a register that could set

CDF_ERROR(Not implemented at the current time – we also have the option to use a mask error bit to disable).
The Error Links bit will be set while one of the Links(fibers) is producing a RX_ER or the Error_Links_FE bit is set.
If the data output from the FIFO's are not aligned properly(Beam_Zero marker, Time_Zero marker and Group Identifier do not match between the six FIFO's) an Alingment_error is generated. This error will cause the same results as the Full Error, the Alingment error signal is also sent to the next stage of the Finder algorithim along with the data from that event.
If one of the FIFO's run out of data before the other FIFOs do then they will also get reset – the outputs become misaligned because the last word out of the FIFO is always being compared and if it's empty the output will not change from the empty FIFO(this may happen if a link has an error – the slice isn't written and one of the FIFOs will run out before the others).

A fiber disable function(register) has been added to mask off the data from a fiber from appearing in the alignment section and the FIFO empty or full section. In reality it should be called Input FIFO disable instead of fiber disable. The data can still arrive on the Fiber but it's not written into the FIFO and the data from the FIFO is not used in the Alignment section that checks the FIFO's for data or for errors. The 10 Cell designs now have the middle two FIFOs or fibers disabled(v6r1). So if a Fiber, TDC, TX or Rx mezzanine board is defective the data from that defective part will not be used to align an event. The data from that fiber will be off or low.

So in summary: data(slices) can only enter the Input FIFO if it is valid and came in a particular order. Data out of a FIFO will need to be aligned or an error is generated. If a link produces an error it will cause the FIFO to be reset which will clear the FIFO, causing that event to be flagged and possibly causing the next event to be missed.
If the error occurred on one of the later slices by the time it was read out of the FIFO some slices of the next event could already be stored in the FIFO. The next events slices that were already stored would be cleared.
I believe that it takes about 3 slices for the FIFO to say that it has data(to enable the read). There will be some latency between all the links.



Yellow trace is the Input aligned signal out of the Input Alignment block

Green trace is the Data valid signal that is produced by the SERDES part

Purple trace is the Data valid signal that travels with the data to the next function in the Finder Algorithim

Red trace represents the first slice of data out of the Input Alignment block for an event

Light Blue trace represents the last slice of data out of the Input Alignment block for an event

There are 24 slices of data in an event.

The Delta time value of 175.32ns is the time that is required by the Input Alignment block within the Stereo Finder FPGA. The Solid orange line is postioned at the farthest left location of all the 6 channels Data Valid signal. For the six fibers that were used in this measurement there was 31ns of latency between them.

The time required by the Input alignment block in the Stereo Finder FPGA was measured to be 150ns-183ns in the teststand, this was with the 6 fibers data valid being within 32ns of each other. Calculated time was determined to be 122ns-185ns, this was done by adjusting the latency between the data to the FPGA that represents the Fiber data and the clock phases.